IN THE CLAIMS

1. (Twice Amended) In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

B3

a conduit for molecules of an inert gas,

a first electrode biased to a first voltage and spaced from the wafer,

a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and the wafer and further spaced from the wafer than the first electrode,

magnetic members providing a magnetic field,

the first electrode and the magnetic members being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas, and

the second electrode and the wafer being disposed relative to each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at a low and controlled speed.

2. (Amended) In a combination as set forth in claim 1,

a first member disposed adjacent the first electrode for providing a reference potential different from the bias on the first electrode to create a first electrical field, and

a second member disposed adjacent the second electrode for providing the reference potential to create a second electrical field,

the first electrical field and the magnetic field being disposed relative to each other and to the molecules of the inert gas from the supply for ionizing the molecules of the inert gas,

the second electrical field and the magnetic field being disposed relative to each other and to the ions of the inert gas to obtain the movement of the ions to the wafer at the low and controlled speed,

the second electrode being contiguous to, but spaced from, the wafer.

3. (Amended) In a combination as set forth in claim 1,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

B3 a+ a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the bias on the first electrode being less than the bias on the second electrode.

8. (Amended) In a combination as set forth in claim 7,

an opening in the enclosure for the flow of the molecules and ions of the inert gas from the enclosure,

B4 the first source of the alternating voltage being operative to produce a direct voltage of the high magnitude and a negative polarity at the first electrode,

the second source of the alternating voltage being operative to produce a direct voltage of the low magnitude and a negative polarity at the second electrode,

the first electrode being disposed in contiguous, but spaced, relationship to the wafer.

13. (Twice Amended) In a combination as set forth in claim 10,

a first electrical conductor disposed in an adjacent, but spaced, relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor,

a second electrical conductor disposed in an adjacent, but spaced, relationship to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second conductor,

the wafer being disposed in a spaced, but contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

15. (Amended) In a combination as set forth in claim 14,

the first capacitor including a dielectric of the molecules and ions of the inert gas and the second capacitor including a dielectric constituting the insulating layer.

16. (Amended) In a combination as set forth in claim 14,

a first electrically conductive member disposed in an adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member, and

a second electrically conductive member disposed in an adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member.

21. (Twice Amended) In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure

first and second electrodes disposed in the enclosure and displaced from each other and from the wafer for producing electrical fields in the enclosure, and

magnetic members disposed in the enclosure for producing a magnetic field in the enclosure in a direction transverse to the electrical field,

a first voltage source for producing a voltage of a high magnitude in the vicinity of the first electrode to obtain a production of a high electrical field in the enclosure,

a second voltage source for producing a voltage of a low magnitude in the vicinity of the second electrode to obtain a production of a low electrical field in the enclosure, and

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating

layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layer.

25. (Amended) A method as set forth in claim 22 wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak electrical field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the capacitor and a circuit including the capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

26. (Twice Amended) A method as set forth in claim 22 wherein

the capacitor constitutes a first capacitor and wherein

the relatively weak electrical field is defined by the first capacitor and a second capacitor in a series circuit and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and in which the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the first capacitor and to provide the first capacitor with the high impedance and wherein

a second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide the second capacitor with a relatively low impedance in comparison to the high impedance of the first capacitor.

28. (Twice Amended) A method as set forth in claim 26 wherein

the wafer is disposed in the relatively weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially through positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through positions in the relatively weak electrical field to facilitate a substantially uniform etching of the surface of the insulating layer on the wafer by the ions and wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the first capacitor and a circuit including the second capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

29. (Twice Amended) A method as set forth in claim 26 wherein

the capacitor constitutes a first capacitor and wherein

the first capacitor and a second capacitor are in series and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and wherein

the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the capacitor and to provide the high impedance and wherein

the second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide a relatively low impedance in comparison to the high impedance of the first capacitor and wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively weak electrical field is provided by a second electrode and by a second alternating voltage providing a relatively low negative bias on the second electrode.

42. (Twice Amended) A method as set forth in claim 37 including the steps of:

introducing an alternating voltage of a first particular magnitude to the first electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

introducing an alternating voltage of a second particular magnitude less than the first particular magnitude to the second electrode to produce a weak negative DC bias on the second electrode for the creation of the weak electrical field, and

providing a high impedance between the second electrode and the wafer and a low impedance between the wafer and the charged particles near the wafer to produce a transfer of charged particles with limited energy to the surface of the insulating layer and the walls of the socket in the insulating layer and to provide the weak and

controlled etching of the surface of the insulating layer and the walls of the socket with a substantially uniform thickness of material from the insulating layer and the wall of the socket without pitting the surface of the insulating layer or the walls of the socket.

43. (Twice Amended) In a combination as set forth in claim 21 wherein,

the first electrode provides the high electrical field in cooperation with the magnetic field for producing an ionization of molecules of the inert gas in the enclosure and wherein

the second electrode provides the low electrical field in cooperation with the magnetic field for etching the surface of the insulating layer on the wafer to obtain the smooth and uniform etching on the surface of the insulating layer at the low rate without any pits in the surface of the insulating layer.

44. (Amended) In a combination as set forth in claim 21 wherein

the first voltage source applies an alternating voltage from the voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the second voltage source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

45. (Amended) In a combination as set forth in claim 21 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

46. (Amended) In a combination as set forth in claim 45 wherein

the first and second electrodes are substantially parallel to the wafer and wherein

the first and second electrical conducting members are substantially parallel to the first and second electrodes.

49. (Amended) In a combination as set forth in claim 47 wherein

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

50. (Amended) In a combination a set forth in claim 44 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

51. (Amended) In a combination as set forth in claim 49 wherein

the first voltage source applies an alternating voltage from the first voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the second voltage source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode and wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the strong electrical field and wherein

a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the weak electrical field.